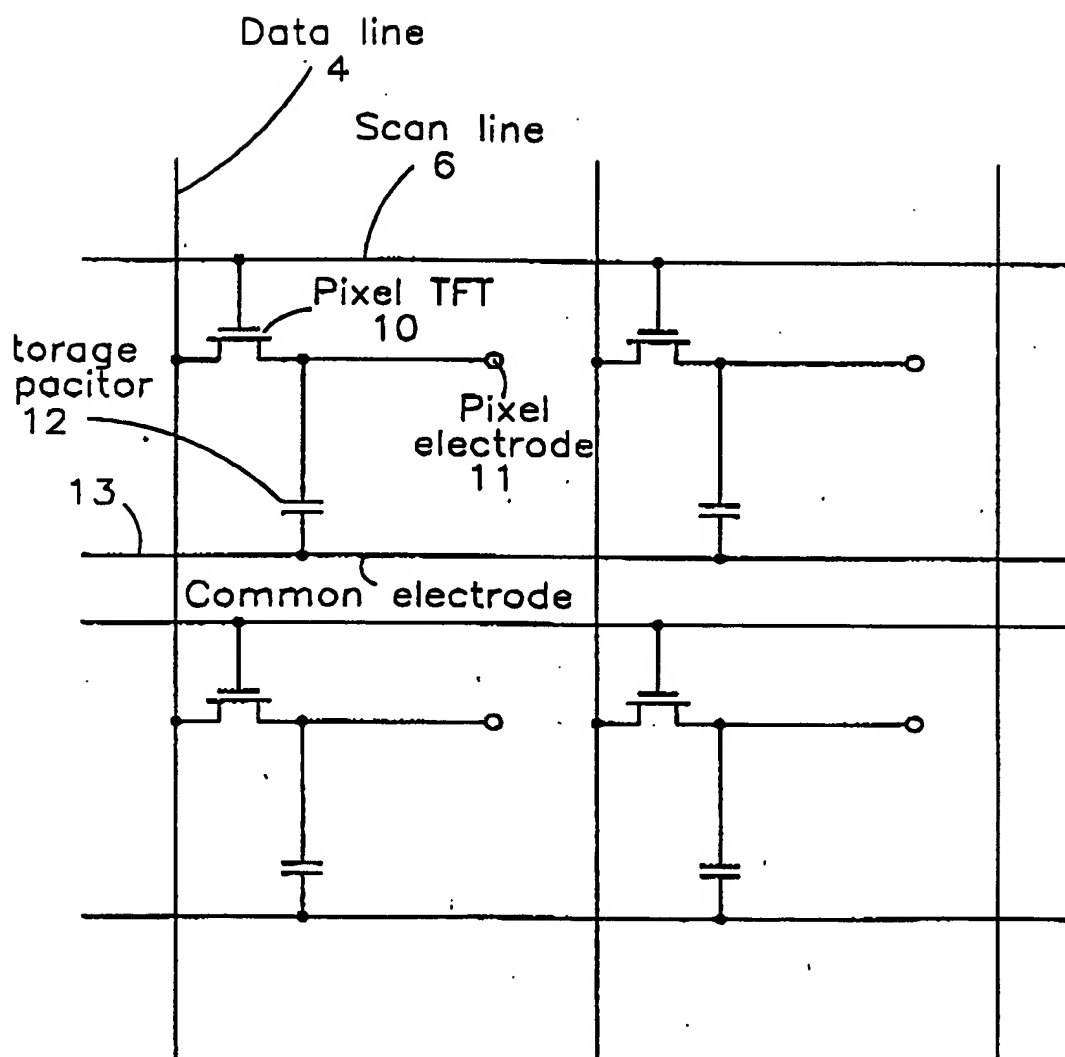
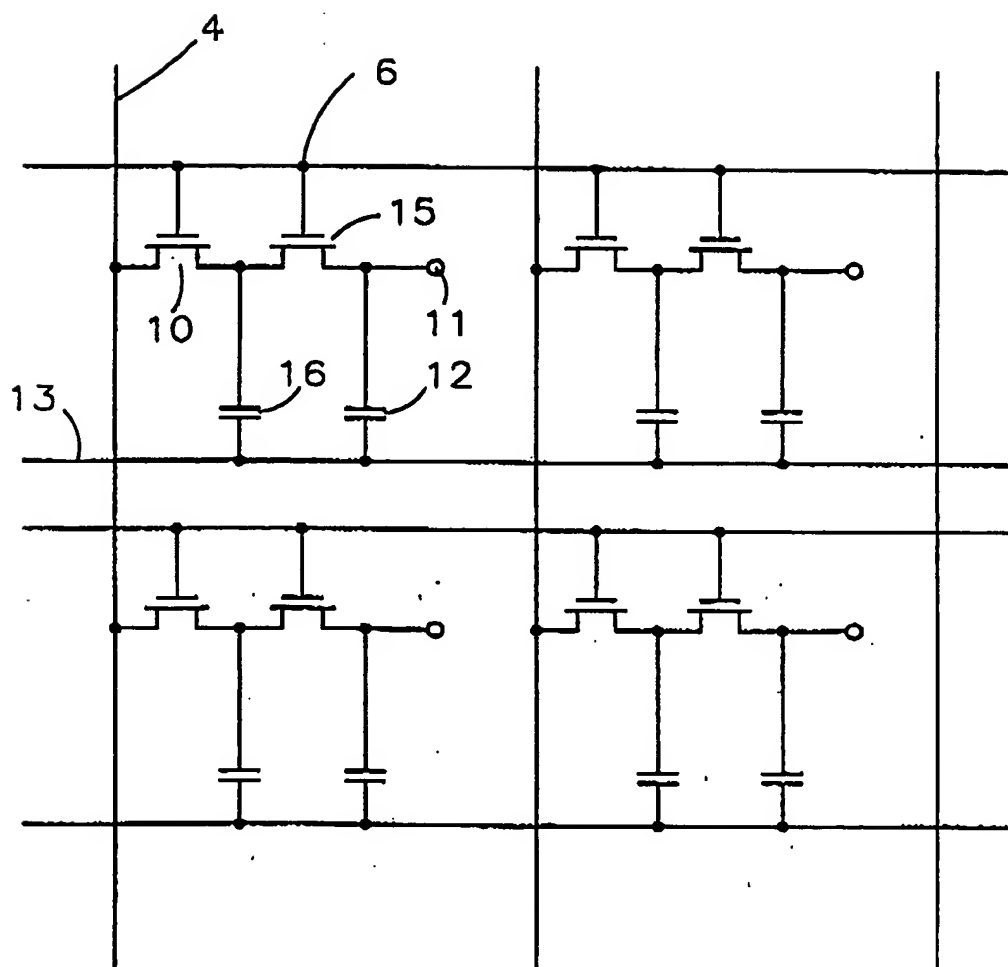
FIG 1

FIG 2

FIG 3

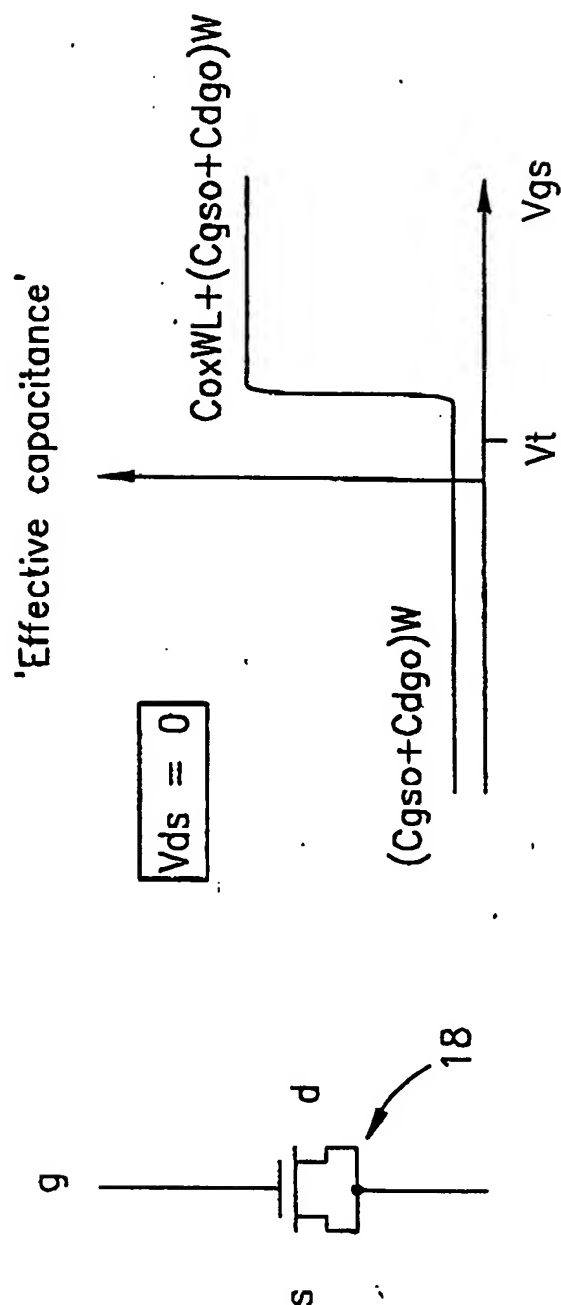
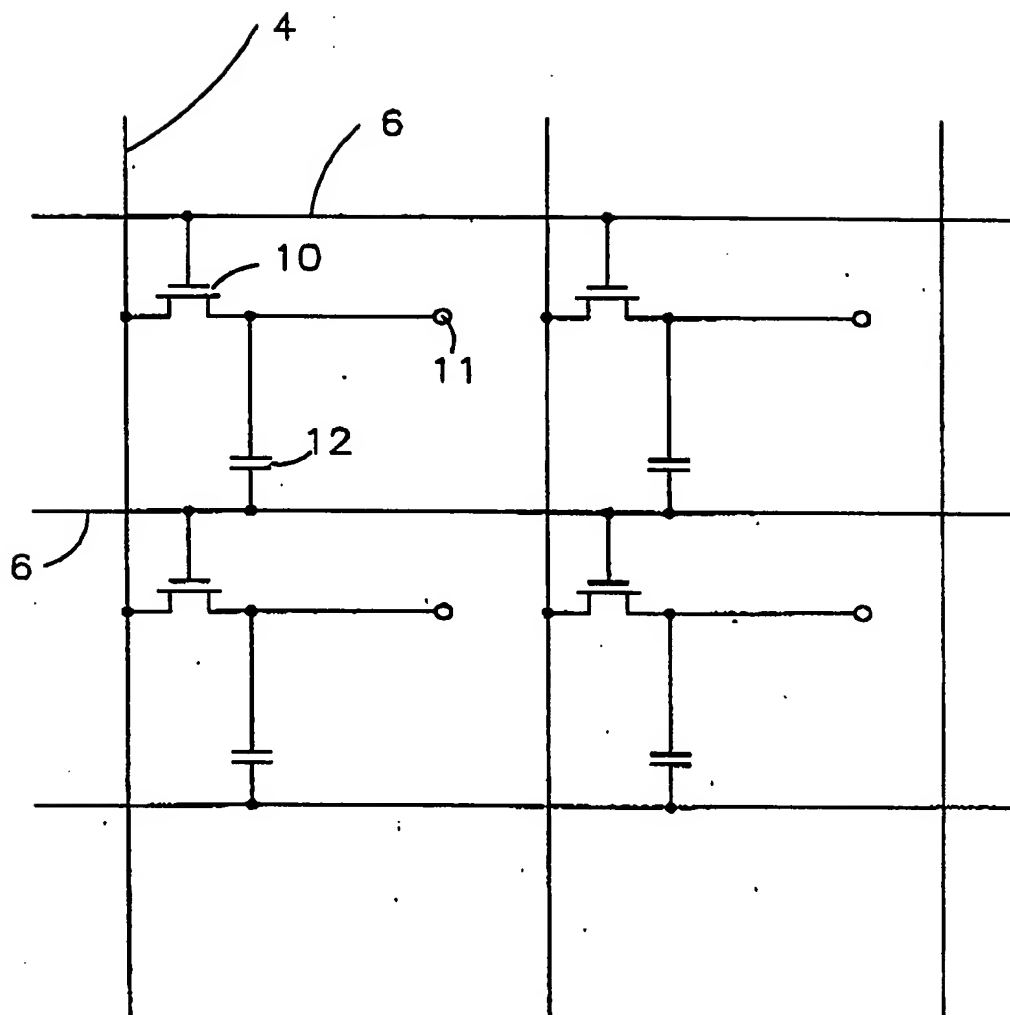
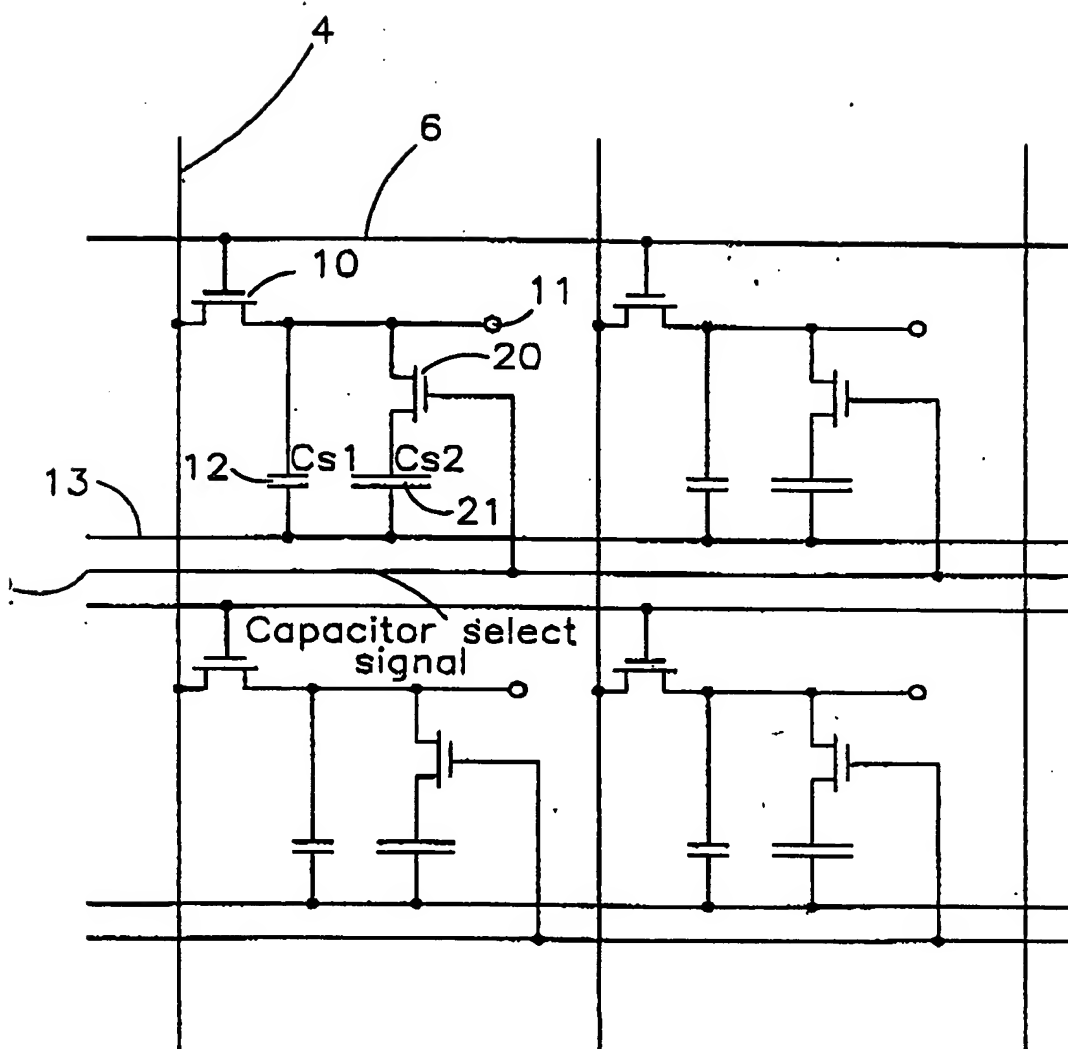


FIG 4

FIG 5

FIG 6

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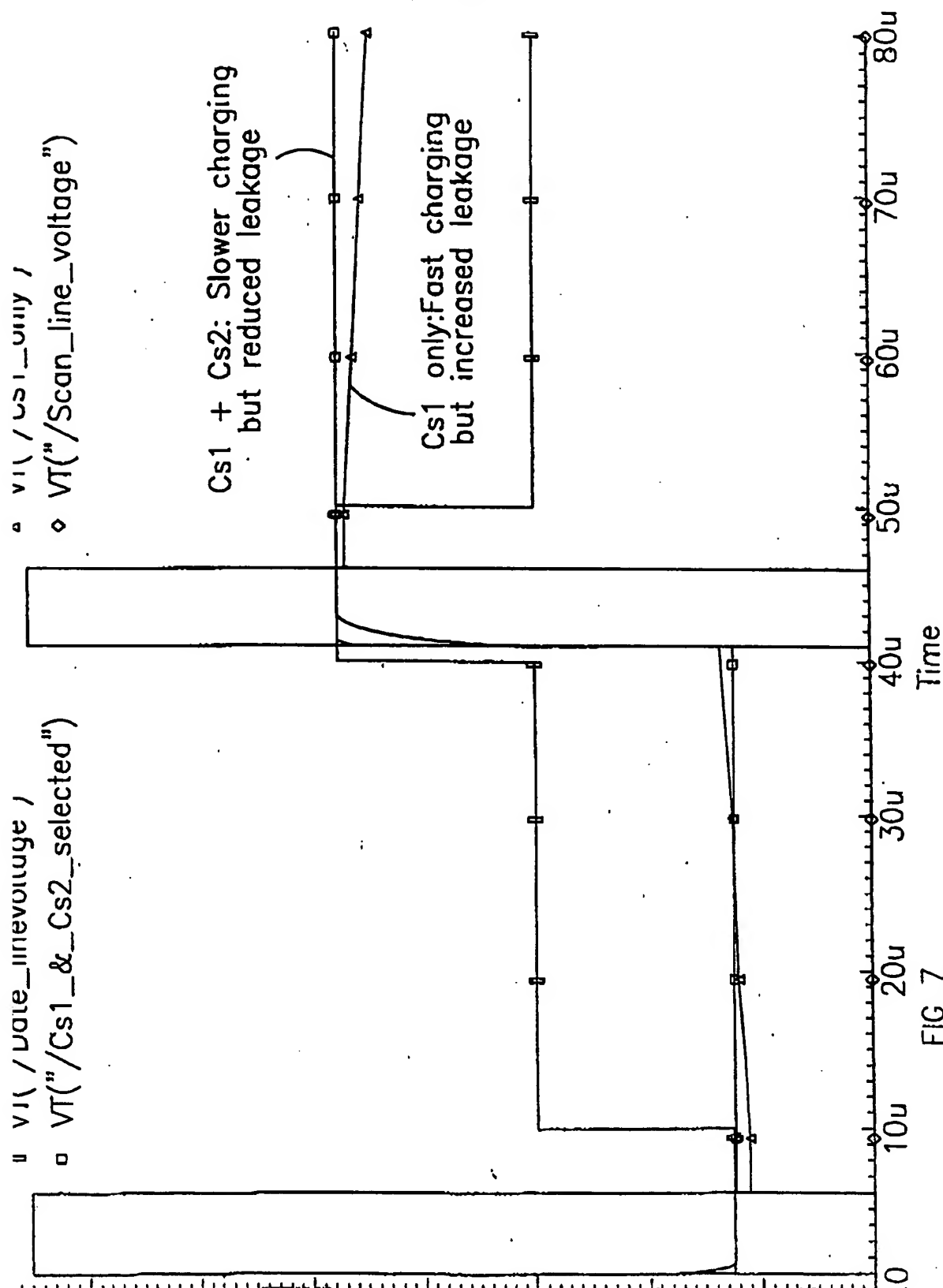


FIG 7

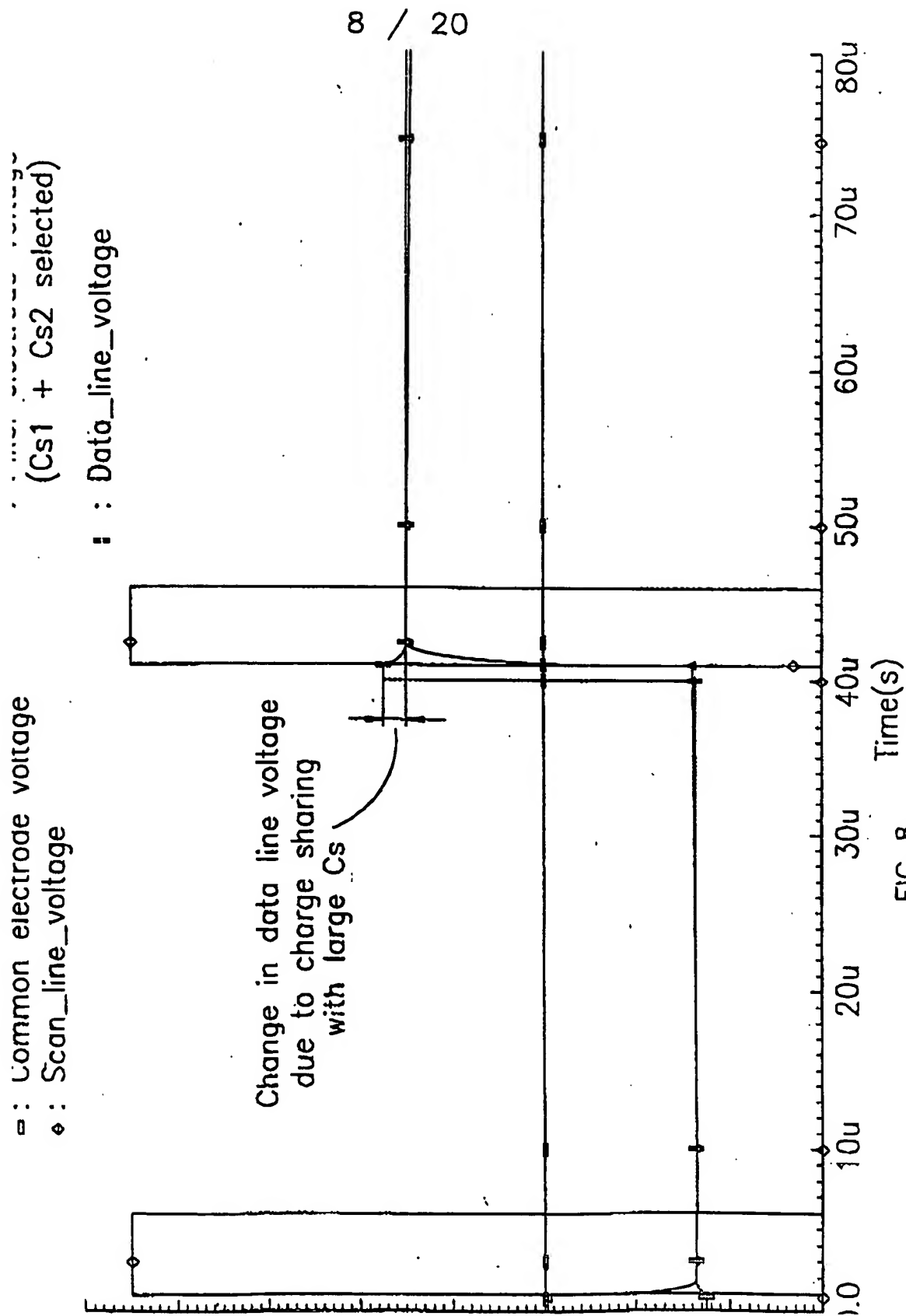
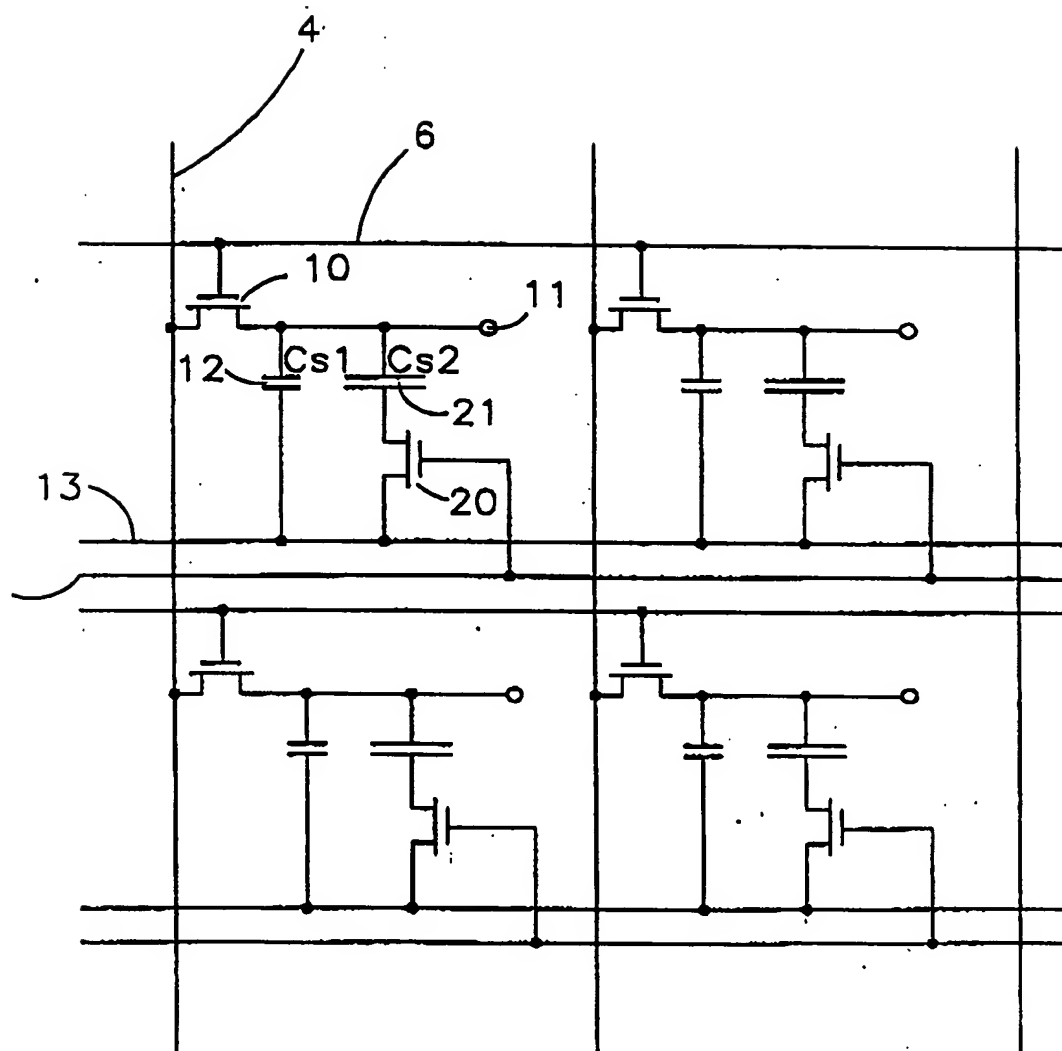
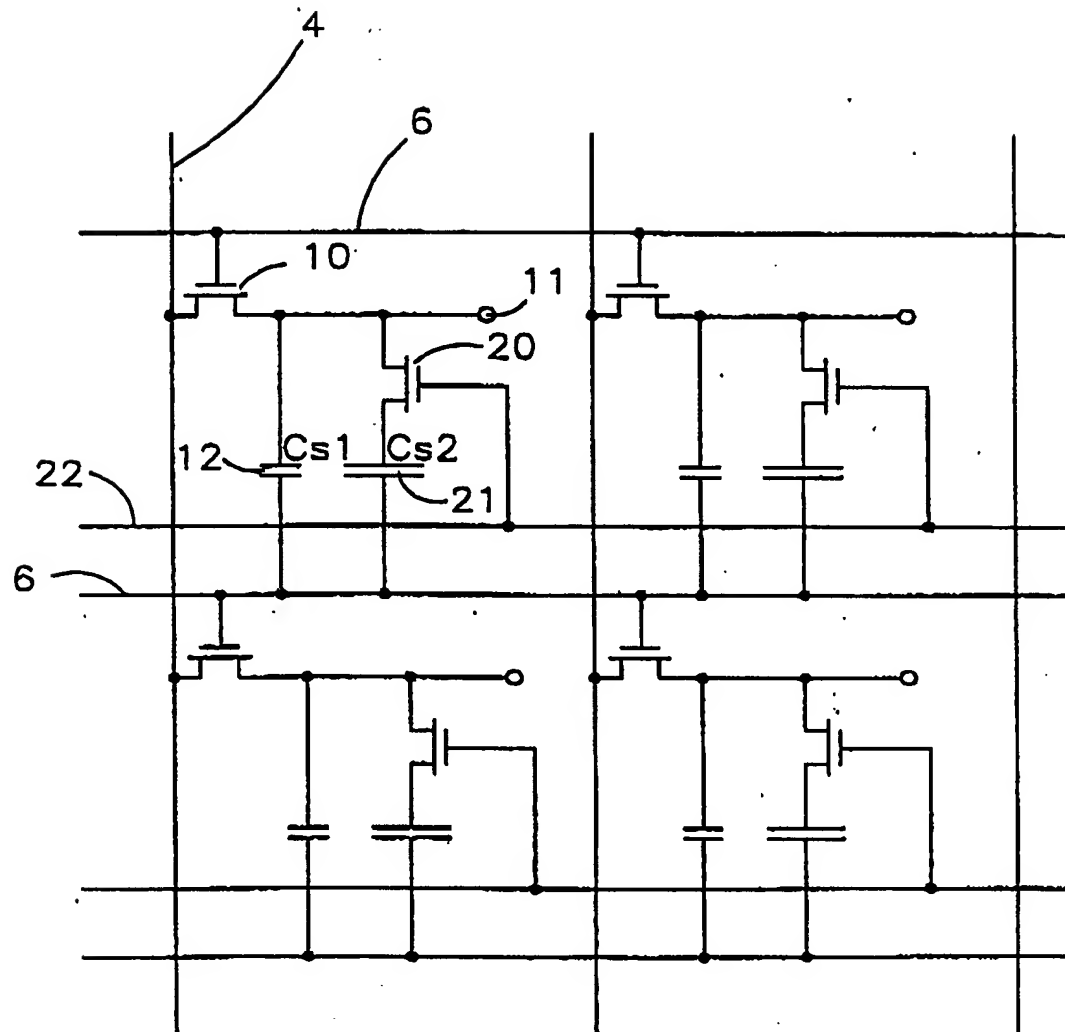
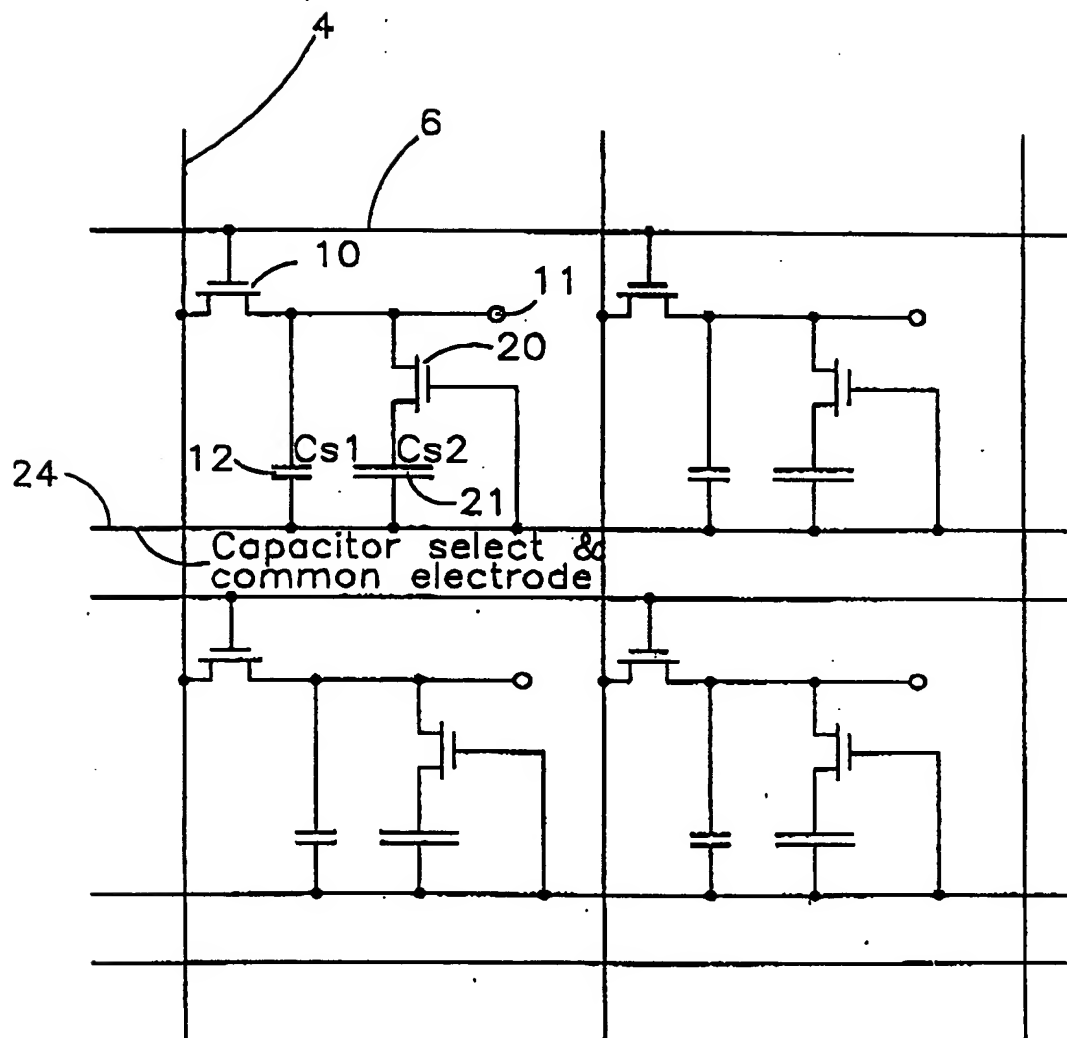


FIG 8

FIG 9

FIG 10

FIG 11

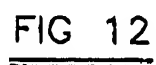
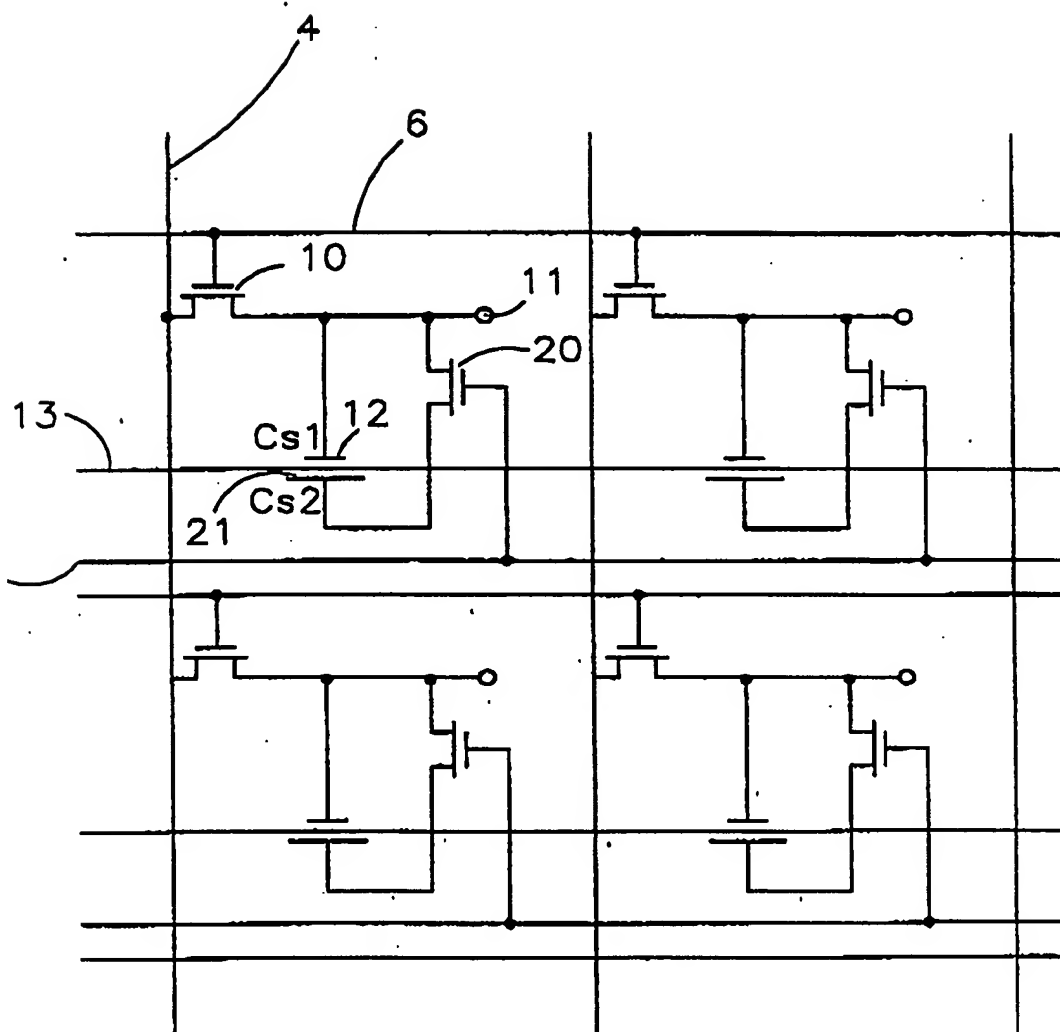


FIG 12

FIG 13

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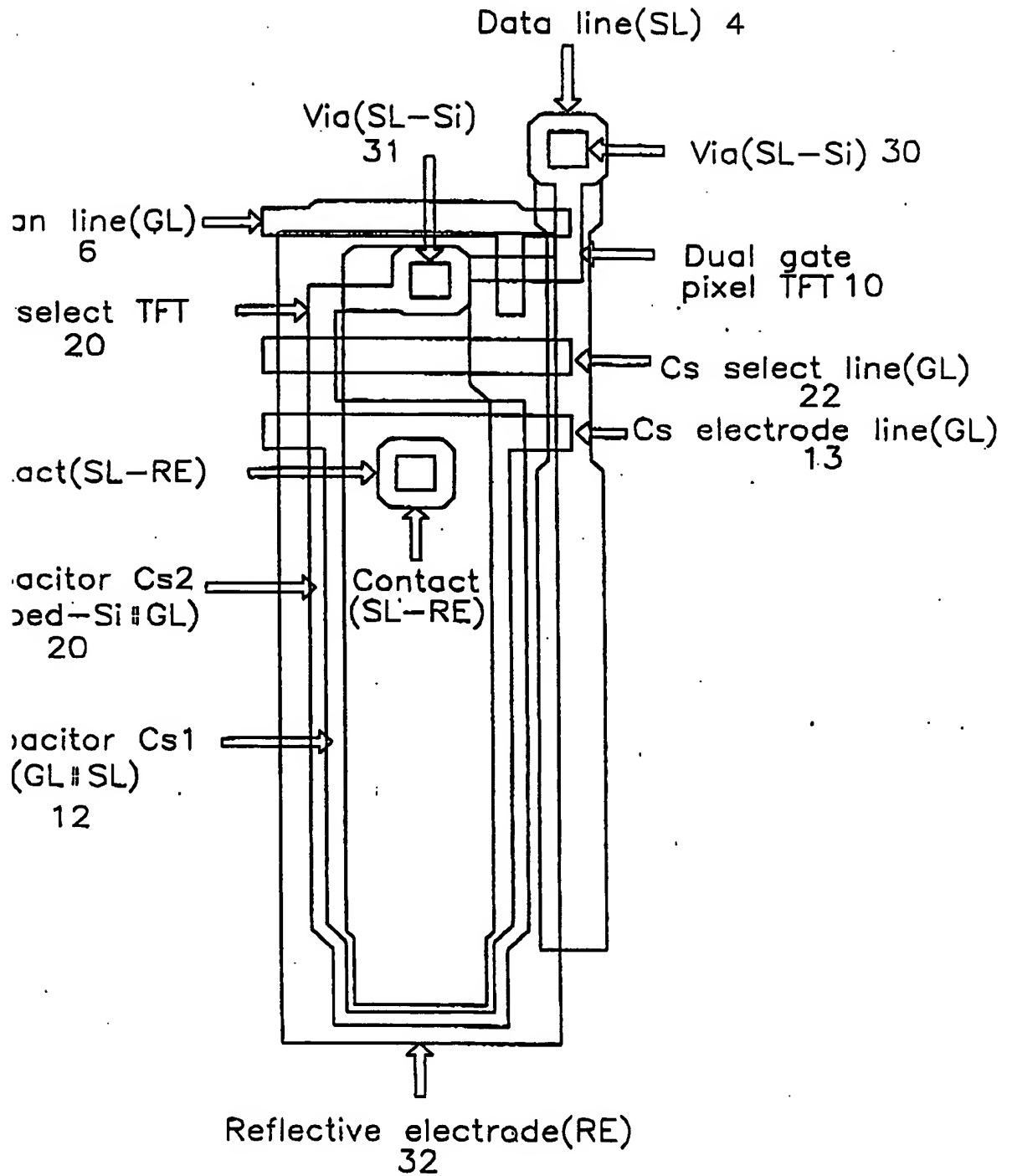
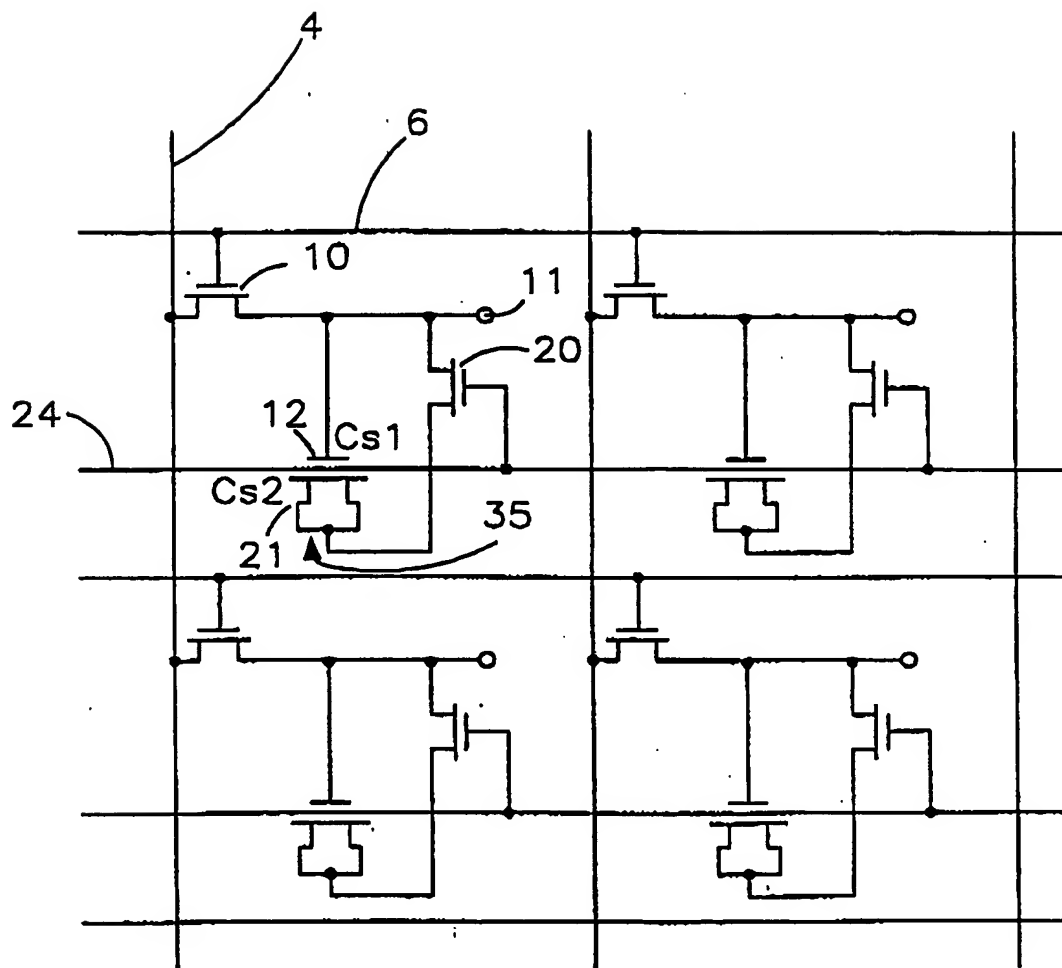


FIG. 14

FIG 15

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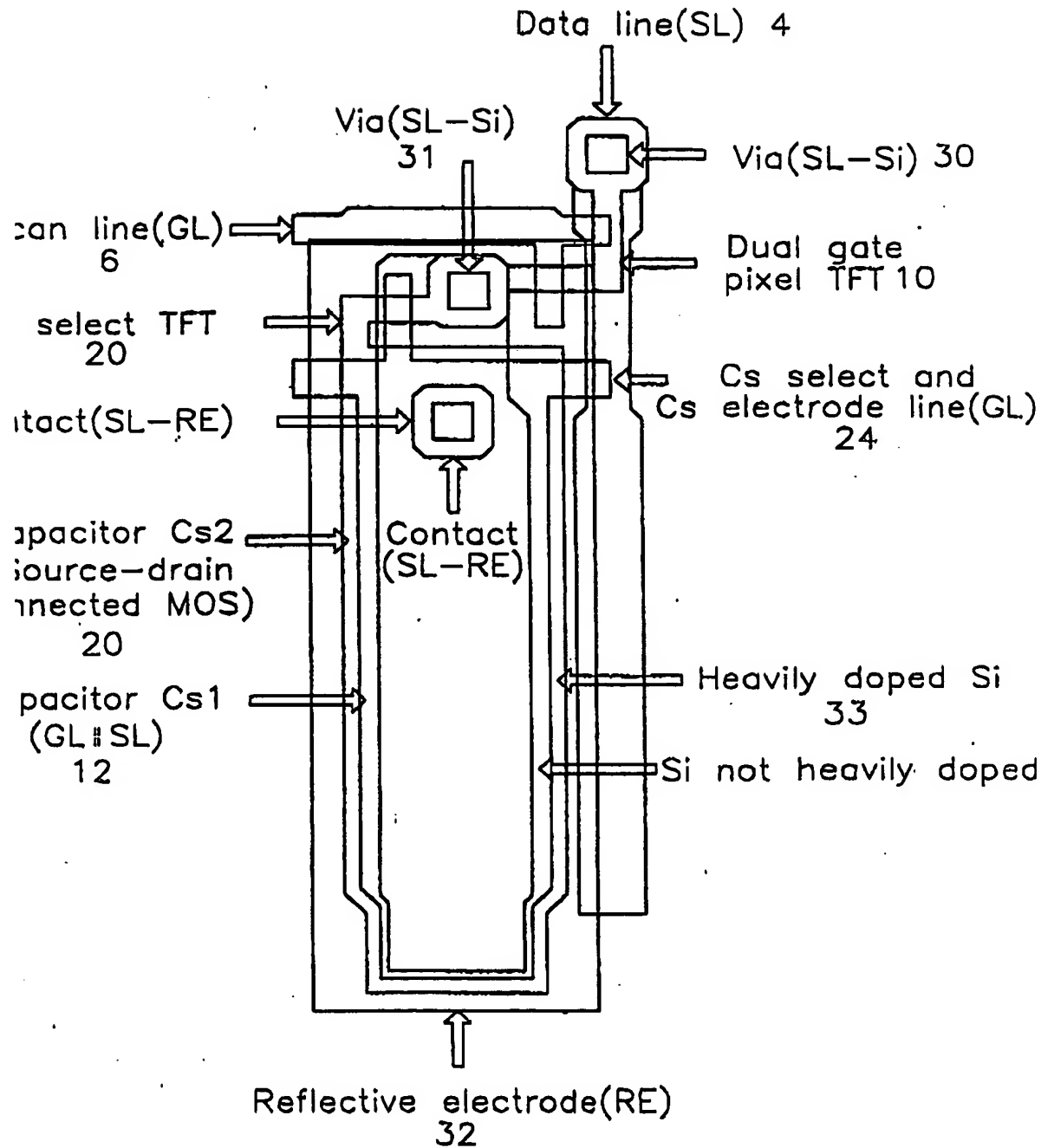
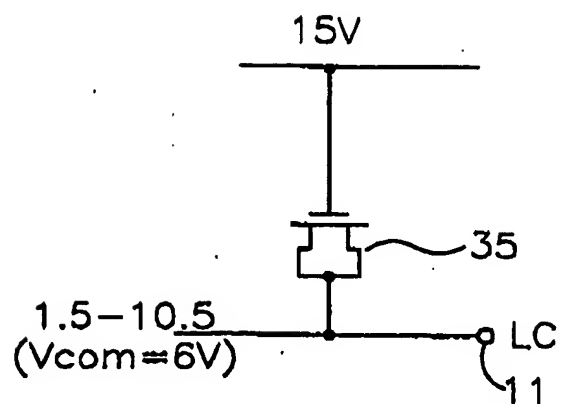
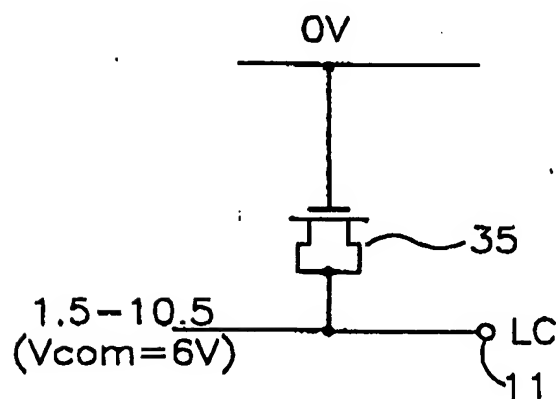


FIG. 16

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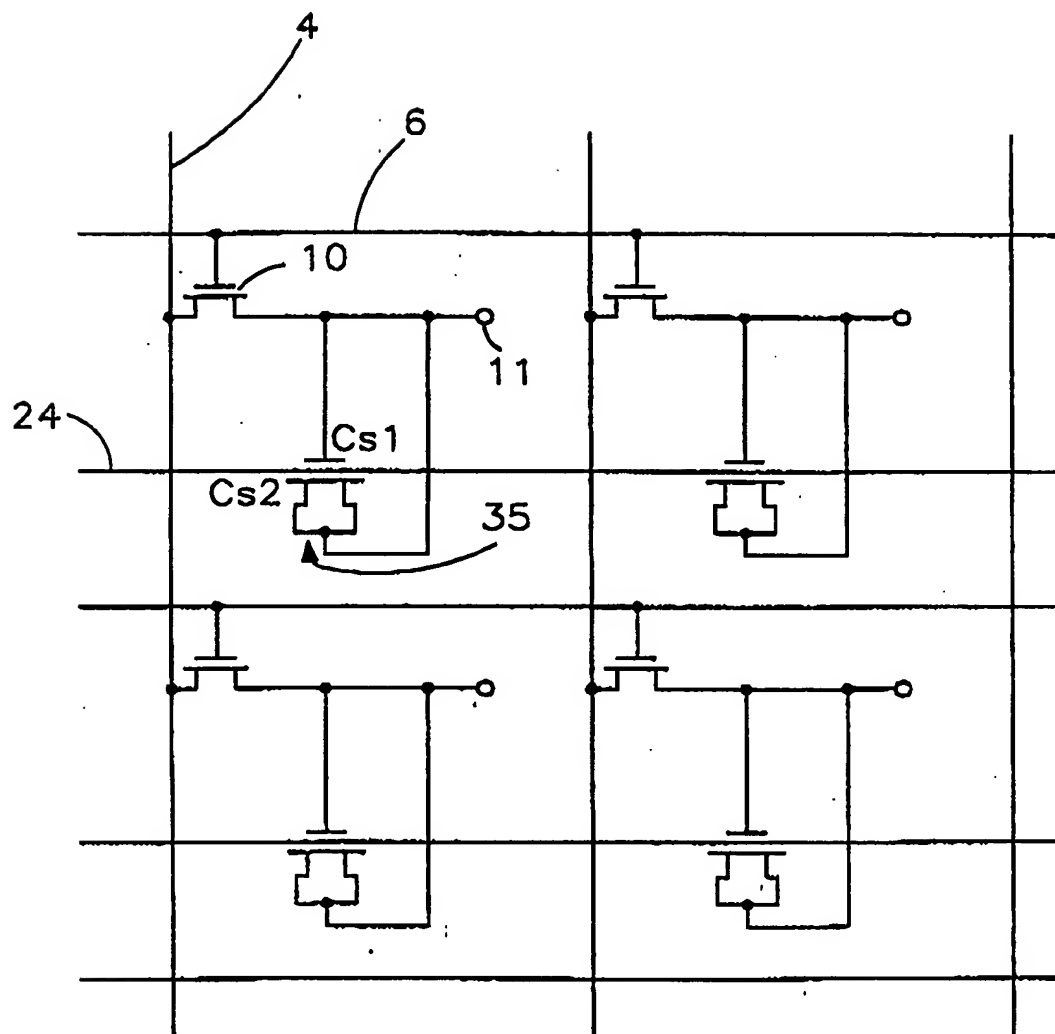


Condition for
high capacitance:
 $V_t < 4.5$



Condition for
low capacitance:
 $V_t > -1.5$

FIG 17

FIG 18

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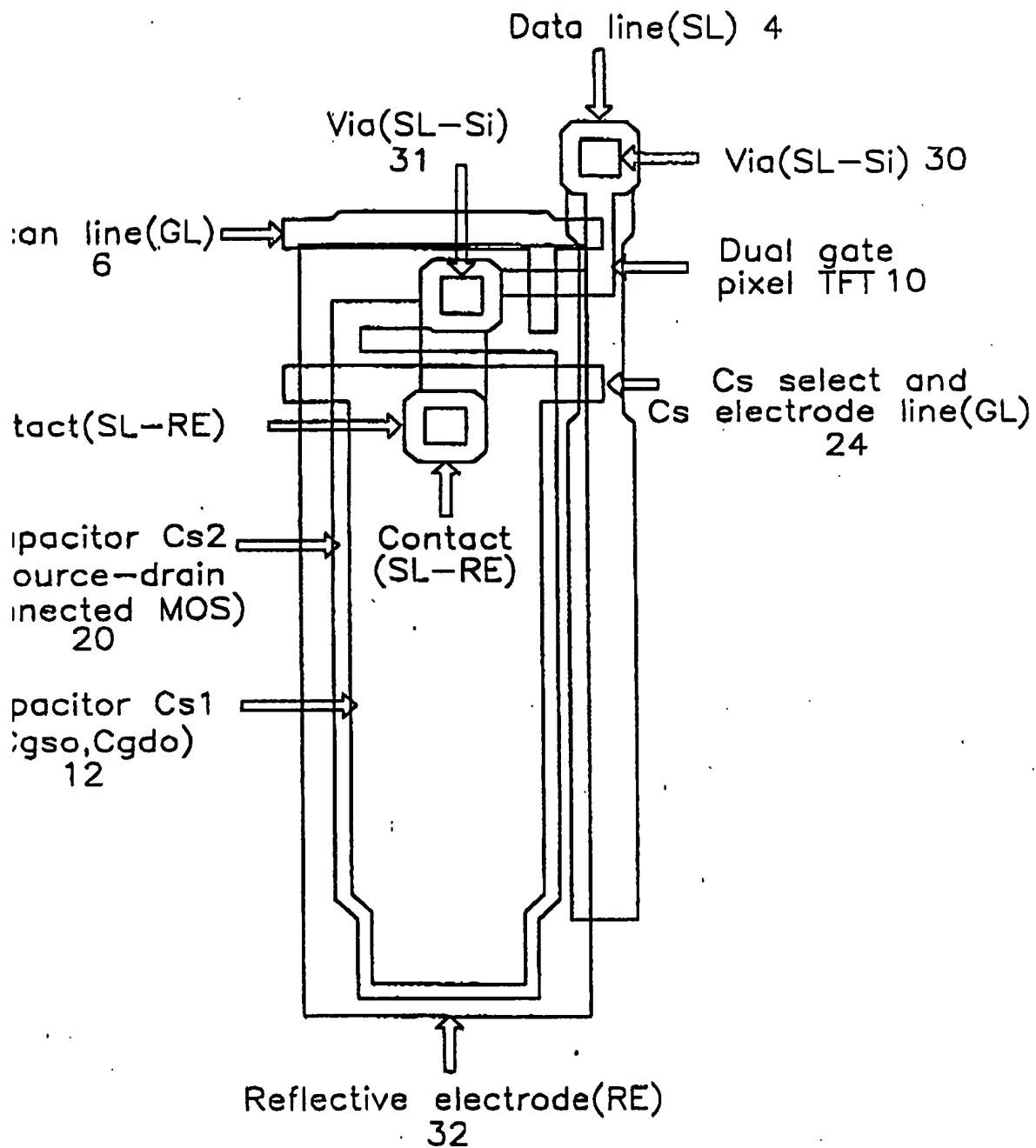
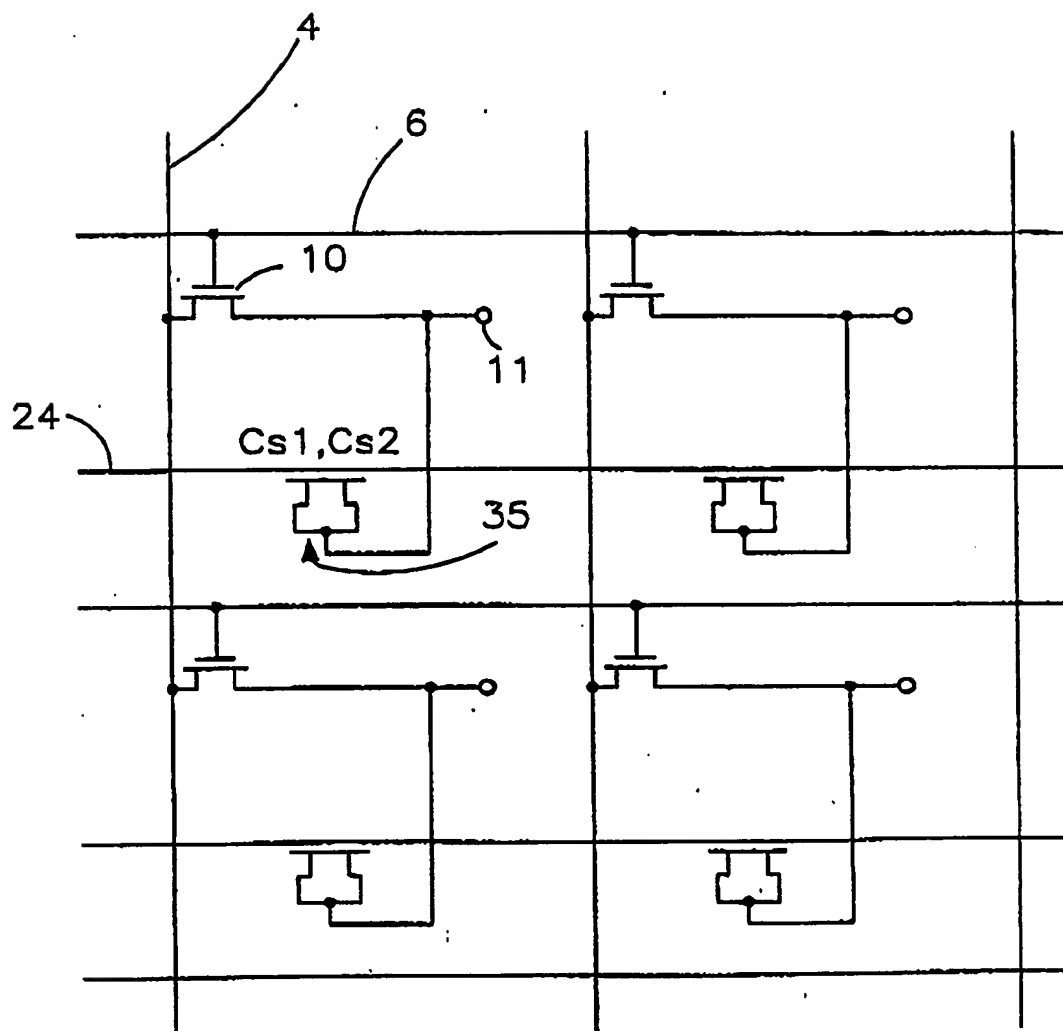


FIG. 10

FIG 20